Tunable Multilevel Storage of Complementary Resistive Switching on Single-Step Formation of ZnO/ZnWO$_x$ Bilayer Structure via Interfacial Engineering

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Ⓢ Supporting Information

ABSTRACT: Tunable multilevel storage of complementary resistive switching (CRS) on single-step formation of ZnO/ZnWO$_x$ bilayer structure via interfacial engineering was demonstrated for the first time. In addition, the performance of the ZnO/ZnWO$_x$-based CRS device with the voltage- and current-sweep modes was demonstrated and investigated in detail. The resistance switching behaviors of the ZnO/ZnWO$_x$ bilayer ReRAM with adjustable RESET-stop voltages was explained using an electrochemical redox reaction model whose electron-hopping activation energies of 28, 40, and 133 meV can be obtained from Arrhenius equation at RESET-stop

voltages of 1.0, 1.3, and 1.5 V, respectively. In the case of the voltage-sweep operation on the ZnO-based CRS device, the maximum array numbers (N) of 9, 15, and 31 at RESET-stop voltages of 1.4, 1.5, and 1.6 V were estimated, while the maximum array numbers increase into 47, 63, and 105 at RESET-stop voltages of 2.0, 2.2, and 2.4 V, operated by the current-sweep mode, respectively. In addition, the endurance tests show a very stable multilevel operation at each RESET-stop voltage under the current-sweep mode.

KEYWORDS: ZnO, interfacial engineering, complementary resistive switching, multilevel storage, current-sweep
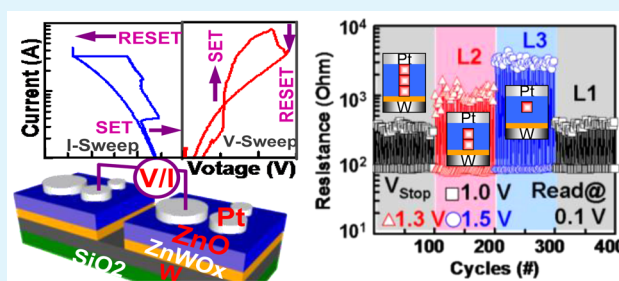
1. INTRODUCTION

Resistive change memory (ReRAM), namely, memristor, is one of the main devices for next-generation nonvolatile memories (NVM) because of its fast switching speed, low power consumption, excellent endurance, and easy integration with current devices. The integration of single memristor into crossbar arrays shows a high-density storage capacity while inducing an inherent problem, namely, the sneak path issue where the leakage current flowing through neighboring ReRAM devices of the crossbar arrays occurs.[1,2] Currently, the reduction of sneak issues are tackled by a memristor connecting with a passive device to control the correct current flow and to prevent misreading under operation, such as one diode—one resistor (1D1R), one transistor—one resistor (1T1R), and one selector—one resistor (1S1R), respectively.[3-6] Alternatively, the complementary resistive switching (CRS) memory has been also proposed to avoid the sneak path for three-dimensional (3D) cross-point configuration by utilizing two bipolar resistive switching memories connected back to back without any switching elements where one cell in the CRS device plays a role of switching resistance, and another cell rectifies sneak path current.[7-9]

In general, different applied bias and polarity of the device enable control of resistance states to define storage signals, resulting in a dramatic enhancement of information storage

density, namely, two resistance levels equal to one bit. As a result, four resistance levels are duplicated to two bits, which correspond to an increase in data stored for the designated ReRAM device. Rozenberg et al. had shown that the storage capacity of one ReRAM device can be obtained up to three bits per cell in 2004.[10] Besides, Tsai et al. had demonstrated HfO$_x$-based ReRAM devices with nearly 1000 times on/off ratio (the resistance ratio between high and low resistance states) and five-level data storage.[11] The storage capacity can be increased by the concept of multilevel storage when the on/off ratio is widened. These results support this multilevel scheme as a robust storage approach for extreme scaling of storage density in ReRAM devices. Usually, multilevel storage can be achieved by either choosing the proper RESET-stop voltage (programming voltage) or by increasing the compliance current (programming current). However, higher compliance current might induce a short circuit because the conductive path is strongly formed and is too difficult to be ruptured. Thus, the functional RESET-stop voltage denotes the better way to widen on/off ratio and further results in multilevel storage. Changing these parameters in different high-resistance state (HRS) must
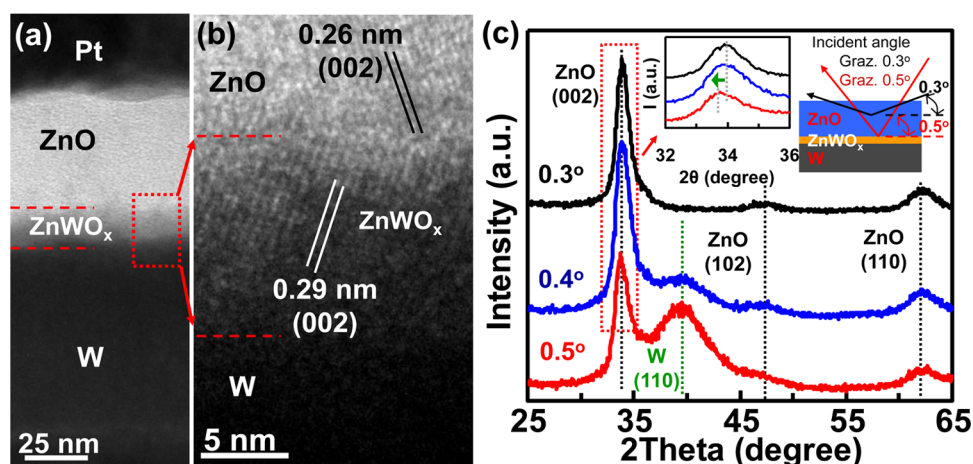
Figure 1. (a) A TEM image of interface between ZnO and ZnWO$_x$. (b) The corresponding high-resolution TEM image taken from rectangular area in (a). (c) GIXRD spectra with different incident angles from 0.3 to 0.5°. (insets) Magnified GIXRD spectra at peak position at ∼34° and schematic illumination of ZnO/ZnWO$_x$/W sample under the GIXRD examination with different grazing angles.

be addressed because each parameter is corresponding to resistance information on the memory.

Furthermore, according to the previous literature, ZnO is one of the most widely investigated materials in electronic and optoelectronic device application including resistive random access memory.[12,13] Among these devices, gas sensors and photodetectors have achieved the outstanding sensitivity significantly benefited from the surface-band bending, which is around 1.53 eV due to the chemisorbed O$_2$ molecules.[14] However, this surface effect is detrimental to some device applications, such as RRAM, because of surface effect-induced electrical instability.[15] Note that the resistive switching mechanism is associated with the formation/rupture of defective-based conductive nanofilaments near the interface between oxide and electrodes, which is enormously influenced by the chemisorbed O$_2$ molecules at the surfaces.[15,16] It leads to the fact that the resistive switching performances of oxide memory devices become sensitive to the ambiences, including switching yield and resistance value fluctuation. Accordingly, it is important to suppress the surface effect on oxide memory switching.

In this paper, we demonstrate a spontaneous formation of ZnO/ZnWO$_x$ bilayer structure via interface engineering for the ReRAM application with multilevel storage operations. In addition, we also demonstrate a concept of multilevel storage of the CRS device. The performances of the ZnO/ZnWO$_x$-based CRS device with the voltage- and current-sweep modes were demonstrated and investigated in detail. Operation under the current-sweep mode in the CRS device can provide the prevention of resistance degradation, especially in the ON state because each high-resistance state can be controlled exactly by the artificially selected specific voltage compliance. The resistive switching behaviors of the ZnO/ZnWO$_x$ bilayer ReRAM with adjustable RESET-stop voltages was explained using an electrochemical redox reaction model whose electron-hopping activation energies can be obtained from an Arrhenius equation at different RESET-stop voltages. Furthermore, maximum array numbers (N) on the ZnO-based CRS device operated by the current-sweep mode can be enhanced, compared with the same device operated by the voltage-sweep mode. Finally, the endurance tests show a very stable multilevel operation at each RESET-stop voltage under the current-sweep mode. The results demonstrate a promising potential of tunable multilevel

storage of CRS device based on single-step formation of ZnO/ZnWO$_x$ bilayer structure via interfacial engineering for the 3D crossbar arrays and also provide an opportunity for all ZnO-based memory system at low temperature process.

2. EXPERIMENTAL SECTION

2.1. Fabrication of Devices. A radio frequency (rf) magnetron sputtering system was used to prepare the devices with the multilayer structure of Pt/ZnO/ZnWO$_x$/W. The bottom W electrode was deposited with a thickness of 100 nm on the SiO$_2$/Si (100) substrate. Subsequently, 25 nm-thick ZnO film was deposited upon the W layer at room temperature with a power density of 2 W/cm^2 and a working pressure of 5 mTorr, respectively. During the sputtering process, the ZnWO$_x$ interfacial layer could be formed simultaneously. Top electrodes were deposited and patterned on ZnO films by a shadow mask with the diameter of 200 μm.

2.2. Characterization. The crystalline structure and nanostructure of the Pt/ZnO/ZnWO$_x$/W device were examined by grazing incidence angle X-ray diffractometer (GIXRD, RIGAKU TTRAX III) and field emission transmission electron microscopy (FE-TEM, JEM-3000F, JEOL operated at 300 kV with point-to-point resolution of 0.17 nm), respectively. Keithley 4200 semiconductor parameter analyzer under DC sweeping mode was used to measure I−V characteristics of devices. During voltage-sweep mode, the positive bias was defined as the current flowed from the top to the bottom electrodes. All of the operation voltages were applied on the Pt top electrode, with which the W bottom electrode was grounded in the ZnO/ZnWO$_x$ RRAM device. For the I−V measurement of the ZnO-based CRS device, the second Pt electrode was grounded. Note that all devices were operated at room temperature.

3. RESULTS AND DISCUSSION

To fabricate the device, ZnO thin film with a thickness of 25 nm was deposited on a W (100 nm)/Pt(100 nm)/SiO$_2$(400 nm)/Si substrate. Pt metal was deposited at room temperature as the top electrode by an rf magnetron sputter. Note that a very thin interfacial layer, namely, the ZnWO$_x$ layer with a thickness of ∼15 nm could be simultaneously formed beneath the ZnO film by ion plasma bombardment phenomenon during sputtering process.[17] A cross-sectional transmission electron microscope (TEM) image of the ZnO/ZnWO$_x$ interface as shown in Figure 1a distinctly confirms the ∼15 nm thick ZnWO$_x$ layer on top of the W layer. In addition, the corresponding high-resolution TEM image of ZnO and ZnWO$_x$ layers taken from the square area in Figure 1a are

shown in Figure 1b, for which internal lattice spacings of 0.26 and 0.29 nm were identified, corresponding to ZnO (002) and ZnWO$_x$ (002) plans, respectively. The enlarged lattice spacing of ZnWO$_x$ (0.29 nm) is believed to be due to enlargement of ZnO lattice owing to the doped W atoms in the ZnO lattice. To shed light on this part, grazing incidence angle X-ray diffractometer (GIXRD) was used to confirm lattice expansion of the ZnWO$_x$ layer by changing incident angles from 0.3° to 0.5° as shown in inset of Figure 1c. The (002) peak in the ZnO layer was clearly indexed at the incident angle of 0.3°, whereas a very slight shift of the ZnO (002) peak to lower angle was found due to the increase of the lattice constant at the incident angle of 0.4°. The substrate signal can be obtained once the incident angle is over 0.5°. The formation of the ZnWO$_x$ layer most likely results from either the substitutional sites of Zn atoms replaced by W atoms or interstitial sites of the ZnO lattice occupied by W atoms in tetrahedral or octahedral sites. Detailed formation of the ZnWO$_x$ layer has been proposed owing to the chemical reaction of W layer with active O^{2-} ions during the ZnO sputtering process, thereby effectively lowering the absolute Gibbs free energy of WO$_x$, which has been reported elsewhere.[17]

Furthermore, the schematic of the spontaneously formed Pt/ZnO/ZnWO$_x$/W device is shown in Figure 2a, and the corresponding stable resistive switching I−V characteristics by controlling RESET-stop voltages at 1.0, 1.3, and 1.5 V with different resistances in the HRS were measured as shown in Figure 2b. Note that a fixed SET voltage of ∼1.0 V with a compliance current (CC) of 10 mA was applied for each measurement. The higher resistance in the HRS was achieved as the larger RESET-stop voltage was applied. The characteristics of resistive switching are very stable at these three level states (L1, L2, and L3) with endurance tests reaching to ∼100 cycles as shown in Figure 2c. By changing RESET-stop voltages, different high resistance states from L1, L2, L3, and L1 can be stably achieved, with which the multilevel stats of the Pt/ZnO/ZnWO$_x$/W device are reversible.

It is well-known that electric field induces the migration of charged defects (e.g., oxygen vacancies), resulting in formation of conductive filament paths, and the switching mechanism is attributed to electron hopping through the localized state associated with oxygen vacancies. For bipolar resistance switching, a positive polarity bias induces negative oxygen ions to recombine with zinc ions and repels oxygen vacancies to rupture conducting filaments.[18] It means that different electric field induces different dispersion, determining different resistance states and hopping distances. This is why the controlling functional RESET-stop voltage would induce different rupture magnitudes, resulting in different HRSs since conductive filament paths in the present study are most likely due to the migration of oxygen ions, namely, formation of Zn-dominated ZnO$_{1-x}$ and ZnO. In addition, the ZnWO$_x$ layer acts not only as the base layer to increase the resistance of the device at the HRS but also as the reservoir for the supplement of oxygen ions, enabling a stable and recognizable performance.[17] To investigate the resistance switching behaviors of the ZnO/ZnWO$_x$ bilayer ReRAM with adjustable RESET-stop voltages, a hopping conduction mechanism is proposed to describe transport characteristics of carriers hopping a barrier as follows:[19]

$$I = qNav_0 e^{-q\Psi_t/KT} e^{qaE/2aKT}$$

where the N, a, ψ_t, E, v_o, T, and k are numbers of space charge, mean free length of hopping distance, barrier height of hopping, applied electrical field as the device in HRS, intrinsic vibration frequency, absolute temperature, and Boltzmann's constant, respectively. By plotting the logarithm of I as the function of $1/kT$ at applied biases of 0.05, 0.01, 0.15, and 0.2 V corresponding to electrical fields of 20, 40, 60, and 80 kV/cm extracted by the applied biases over the ZnO film thickness of 25 nm in the HRS, the linear slops at RESET-stop voltages from 1 to 1.5 V, representing the barrier height of carrier hopping, ψ_t, can be founded as shown in Figure 3a−c, respectively. The linear behaviors at different applied biases clearly indicate that carriers transported in the ZnO layer are dominated by the hopping process. It can be explained why the barrier height of hopping decreases as the applied field increases. Furthermore, to shed light on characteristics of hopping conduction at different RESET-stop voltages, thermal activation energy (E_a), indicating the correlation of hopping conduction between different RESET-stop voltages and applied electrical field, can be given by an electrochemical redox reaction model in terms of the Arrhenius equation:[19−21]

$$E_a = -\frac{\partial \log I}{\partial\left(\frac{1}{kT}\right)} = E_c - E_f - \frac{qE\Delta z}{2}$$

where E_c, E_f, E, and Δz represent conduction band, Fermi level, applied field, and average hopping distance, respectively. By further plotting $\partial \log I/\partial(1/kT)$ as the function of applied fields (obtained by the applied voltages in HRS over the 25 nm thick ZnO layer), E_a of 28, 40, and 133 meV, indicating the energy
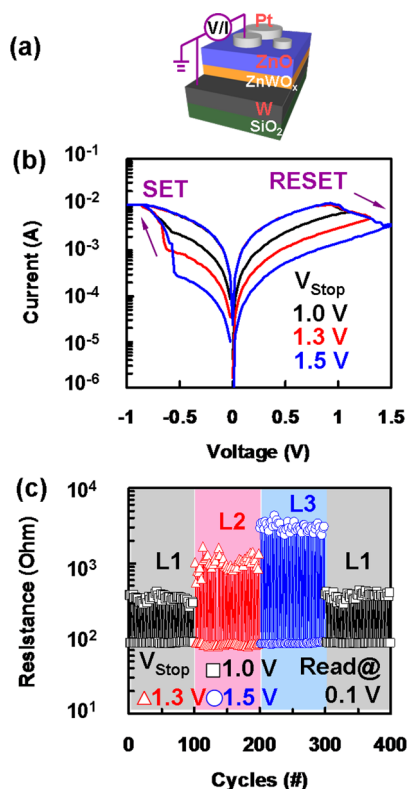
Figure 2. (a) A schematic of the spontaneously formed Pt/ZnO/ZnWO$_x$/W. (b) I−V behaviors of Pt/ZnO/ZnWO$_x$/W device with multilevel storages at RESET-stop voltages of 1, 1.3, and 1.5 V. (c) Endurance test of at least 100 cycles for Pt/ZnO/ZnWO$_x$/W device with different multilevel storages.
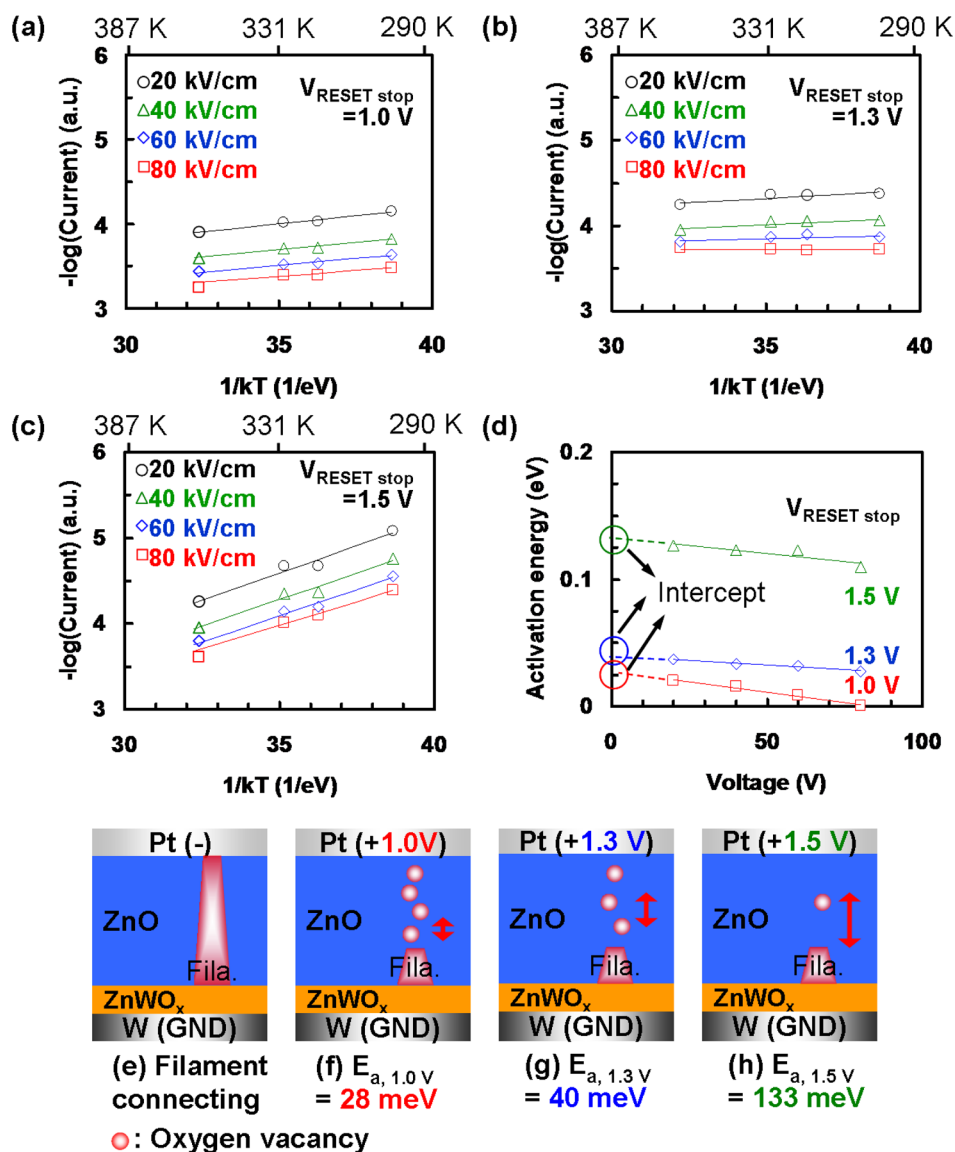
Figure 3. (a−c) The correlation of log(I) vs $1/kT$ at different applied fields and RESRT-stop voltages and activation energy vs applied electrical fields at different RESET-stop voltages. (e−h) The schematic of how different activation energies creased by the RESET-stop voltages influence carriers hopping mechanisms from LRS to HRS, respectively.

barrier for carriers hopping from Fermi levels to conduction bands, can be interpolated from intercepts with the vertical axes at the applied field (voltage) = 0 with different RESET-stop voltages of 1, 1.3, and 1.5 marked by circular points in Figure 3d, respectively. The schematic of how different activation energies created by the RESET-stop voltages influence carriers hopping mechanisms are individually shown in Figure 3e−h. As can be seen from Figure 3e, the device is in low-resistance states (LRS) due to the existence of conduction filaments after a negative bias was applied on the Pt top electrode. Oppositely, a positive bias applied on the Pt top electrode induces oxygen ion migration and repels oxygen vacancies to rupture conductive filaments as shown in Figure 3f. During the "RESET" process, the higher RESET-stop voltage leads to the larger activation energy due to the longer average hopping distance, suggesting the higher resistance in the HRS as shown in Figure 3g,h. This is why the activation energy increases as the RESET-stop voltage increases.

The CRS memory was proposed to avoid the sneak path current for a 3D cross-point configuration application by utilizing the two bipolar resistive memories connected back to back without any switching elements. The CRS concept based on the ZnO/ZnWO$_x$ bilayer memristor by connecting the Pt/ZnO/ZnWO$_x$/W device (A cell) and the inverse W/ZnWO$_x$/ZnO/Pt device (B cell) in series simplistically was demonstrated with direct current (DC) endurance >200 cycles for a possible application in 3D multilayer stacking (Supporting Information, Figure S1), and the detailed operation and switching mechanism of the CRS device was addressed in Supporting Information, Figure S2 and elsewhere.[17] The stable characteristic of the CRS device is most likely from single-step formation of ZnO/ZnWO$_x$ bilayer structure via interfacial engineering. By using the conception of the multilevel states of the Pt/ZnO/ZnWO$_x$/W device, the promising potential of the multilevel in the CRS device can be demonstrated for the first time. To provide four separated resistance levels, each high-resistance level was tuned individually by adjusting the
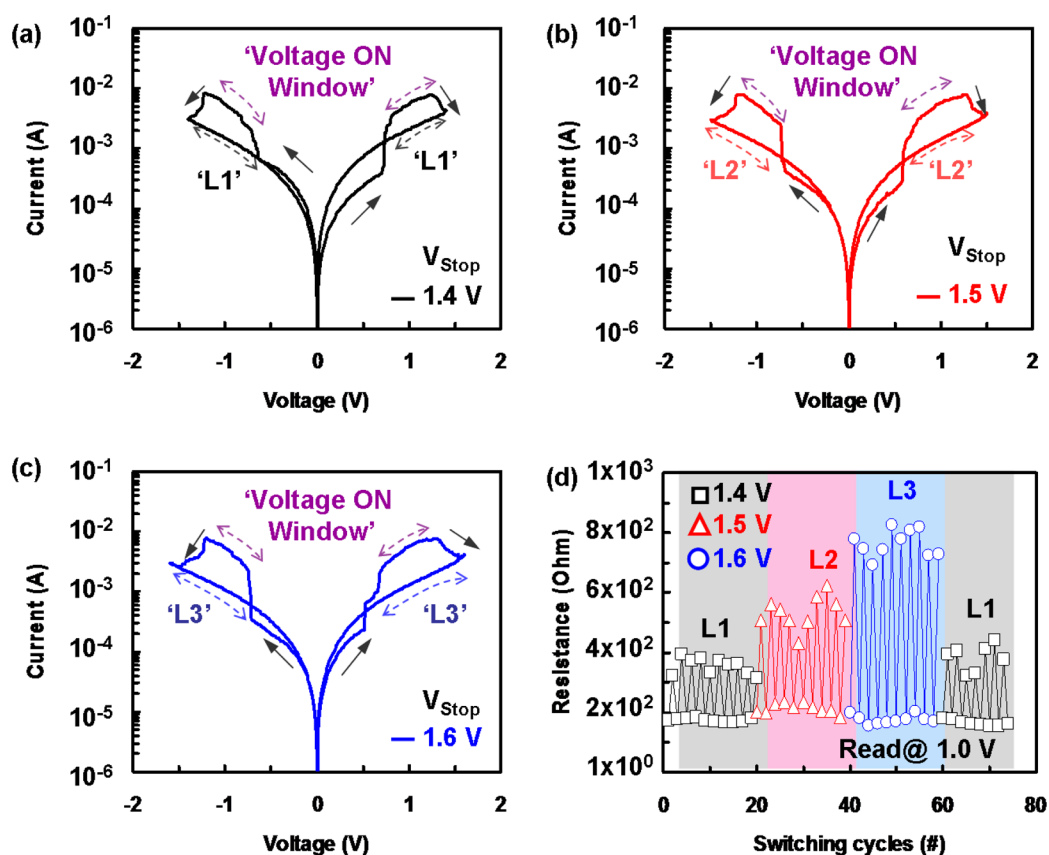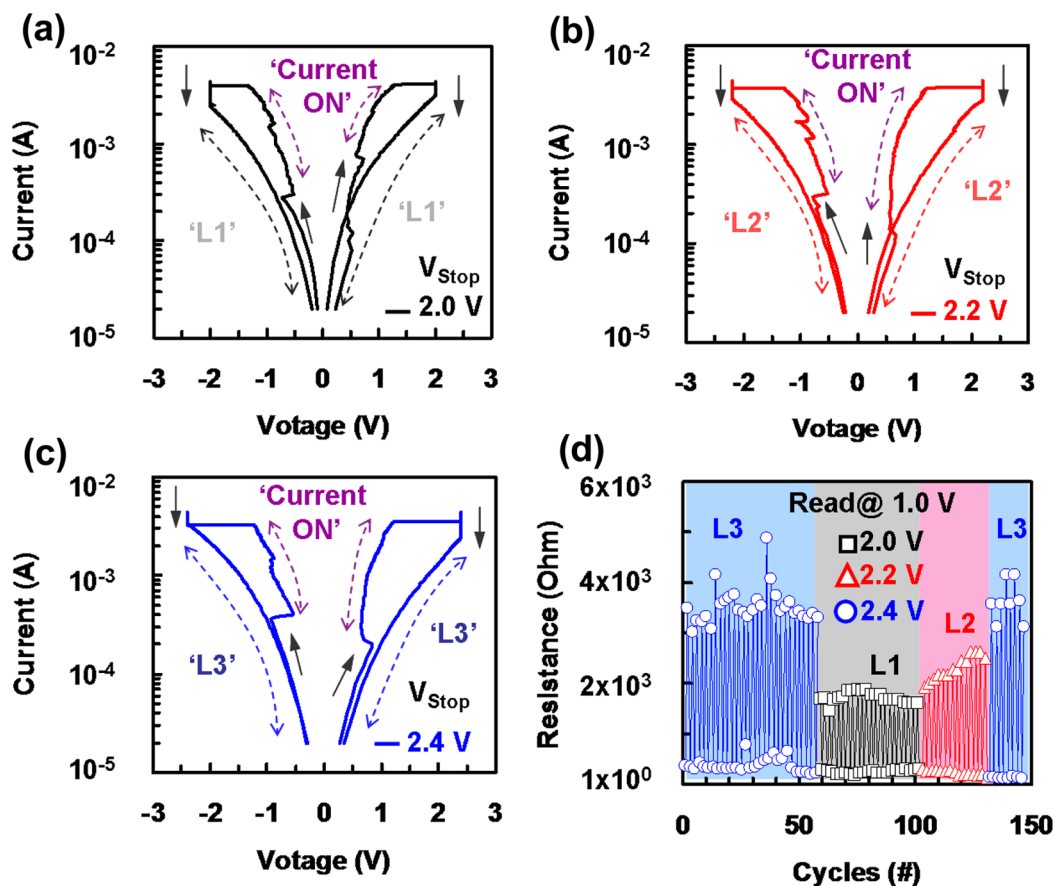
Figure 4. (a−c) Typical semilogarithm scale *I*−*V* curves of CRS device operated by voltage sweep mode with different RESET-stop voltages at 1.4, 1.5, and 1.6 V, respectively. (d) Endurance tests of CRS device with different multilevel storages.

amplitude of the corresponding RESET-stop voltage. To achieve the operation concept, different HRSs of the CRS device at RESET-stop voltages of 1.4, 1.5, and 1.6 V were applied under a voltage-sweep operation mode. The corresponding *I*−*V* characteristics with different resistance stats in the HRS and different "voltage ON window" at different RESET-stop voltages are distinctly shown in Figure 4a−c, respectively. The reversible behaviors of the multilevel CRS were measured at room temperature (Figure 4d); the corresponding HRSs from L3, L1, L2, and L3 with different RESET-stop voltages from 1.4, 1.5, 1.6, and 1.4 V were reversibly demonstrated, respectively. Ideally, the larger the RESET-stop voltage that was applied, the higher the resistance state in the HRS and more broadened "voltage ON window" that can be achieved. However, we find that the "voltage ON window" appears to be a degradation behavior during adjustable multilevel operation no matter what kinds of bias polarities (forward and reverse bias polarities) were applied (Supporting Information, Figure S3). In addition, significant difference in OFF state leads to unstable turn-off voltages in the CRS device during the voltage-sweep mode after several switching cycles. The degraded performance of the multilevel CRS is because one of cells is gradually RESET back to initial resistance state (IRS), harshly inducing the SET process for another cell in the next switching cycle. Therefore, it requires electroforming process again to trigger the resistance returning back to LRS. These unstable switching conditions result from no current compliance to protect devices during the RESET process. However, applying higher RESET-stop voltage to achieve higher HRS to increase on/off ratio might induce

unstable performance and poor endurance because the turn-on voltage is increased when the resistance state of the device approaches the initial state of the device.

To prevent the CRS device switching back to IRS, a current-sweep mode with voltage compliance instead of a voltage-sweep mode was applied to precisely control HRS, leading to more stable multilevel switching in the CRS device. In addition, artificially controlled compliance current in the RESET process can also avoid a short circuit induced by reforming process. The corresponding *I*−*V* characteristics of the CRS device with the current-sweep mode at different RESET-stop voltages of 2, 2.2, and 2.4 are shown in Figure 5a−c, respectively. Obviously, the CRS device with the current sweep operation substantially broadens the "current ON window" by increasing RESET-stop voltage and further prevents demand of the extra electroforming process. It is believed that the unstable performance of CRS device mainly results from presence of power stress overshooting effect during the voltage sweep mode in the nonswitching cell.[22] However, such unstable power stress can be significantly reduced by the operation of current-sweep mode with a voltage compliance. The endurance tests with three reversible HRS states are measured at room temperature in Figure 5d, confirming a very stable multilevel operation with DC endurance results of at least 50 cycles at each RESET-stop voltage under the current-sweep mode. In addition, the measured values of resistance in the HRS were increased from 1.8 to 3.6 kΩ with the increase of RESET-stop voltages from 2.0 to 2.4 V, respectively.

To estimate the maximum array density of the CRS device, the worst-read scheme was employed in assuming $N \times N$

Figure 5. (a−c) Typical semilogarithm scale $I-V$ curves of CRS device operated by current-sweep mode with different RESET-stop voltages at 2.0, 2.2, and 2.4 V, respectively. (d) Endurance tests of CRS device with different multilevel storages.

crossbar arrays that can be simplified as the equivalent circuit as shown in Supporting Information, Figure S4. The method of accessing the crossbar is to select one word-line, pull up one bit-line, and leave the other bit-lines floating, resulting in less power consumption. The method allows only the bit-line and word-line connected with the selected cell to be pulled up and grounded, respectively. For the higher ON/OFF ratio, the RESET-stop voltages were from 1.4 to 1.6 V and from 2 to 2.4 V for the multilevel storage CRS devices operated by the voltage-sweep and current-sweep modes, respectively. The defined read margin, (ΔV_{out}) normalized to pull-up voltage (V_{pu}), could be expressed as follows:[23,24]

$$\frac{\Delta V_{\text{out}}}{V_{\text{pu}}} = R_{\text{pu}} \times \left\{ \left[\left(\frac{R_{\text{LRS}}^{\text{select}} \times \frac{2R_{\text{LRS}}^{\text{sneak}}}{N-1}}{R_{\text{LRS}}^{\text{select}} + \frac{2R_{\text{LRS}}^{\text{sneak}}}{N-1}} \right) + R_{\text{pu}} \right]^{-1} \right.$$

$$\left. - \left[\left(\frac{R_{\text{HRS}}^{\text{select}} \times \frac{2R_{\text{LRS}}^{\text{sneak}}}{N-1}}{R_{\text{HRS}}^{\text{select}} + \frac{2R_{\text{LRS}}^{\text{sneak}}}{N-1}} \right) + R_{\text{pu}} \right]^{-1} \right\}$$

where the R^{select}, R^{sneak}, R_{pu}, are parameters of selected cell resistance, sneak path resistance, and connective resistance in measured system, respectively. Table 1 summarizes extracted parameters and calculated maximum array size of the CRS device operated by voltage-sweep and current-sweep modes. The normalized readout margins as a function of the number of word/bit lines for a readout voltage at 1 V in the ZnO/ZnWO$_x$

Table 1. Extracted Parameters and Calculated Maximum Array Size of Pt/ZnO/ZnWO$_x$/W CRS Devices

RESET voltage, V	reading voltage	LR(Ω)[a,b]	HR(Ω)[a,c]	SR(Ω)[a,d]	N with >10% $\Delta V_{\text{out}}/V_{\text{pu}}$
		voltage-sweep mode			
1.4	1	176	355	1429	9
1.5	1	215	535	1989	15
1.6	1	178	766	2398	31
		current-sweep mode			
2.0	1	348	1671	6513	47
2.2	1	241	2215	8607	63
2.4	1	378	3548	8100	105

[a]Resistance was read at the positive side. [b]Low resistive state of select cell (= pull-up resistance) was read at the reading voltage. [c]High-resistive state was read at the reading voltage. [d]Sneak pass resistance was read at the half reading voltage.

bilayer CRS configuration are shown in Figure 6a,b for the voltage-sweep and current-sweep modes, respectively. Obviously, in the case of the voltage-sweep mode, the maximum array numbers (N) are 9, 15, and 31 at RESET-stop voltages of 1.4, 1.5, and 1.6 V by taking $\Delta V/V_{\text{pu}}$ of 0.1 (10%) into account, respectively. However, the maximum array numbers are increased into 47, 63, and 105 at RESET-stop voltages of 2.0, 2.2, and 2.4 V under the current-sweep mode, respectively. The results demonstrate a promising potential of tunable multilevel storage of complementary resistive switching on single-step formation of ZnO/ZnWO$_x$ bilayer structure via interfacial
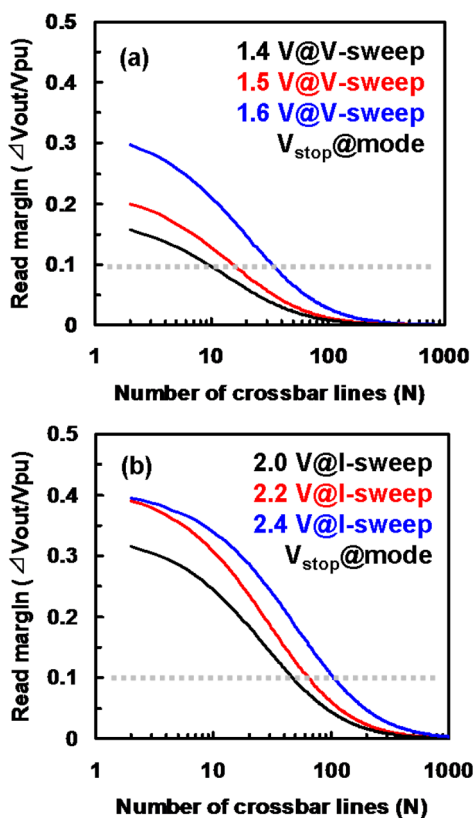
Figure 6. Normalized readout margins as a function of the number of word/bit lines for a readout voltage of 1 V in the ZnO-based CRS configuration operated by (a) voltage-sweep and (b) current-sweep modes at different RESET-stop voltages, respectively.

engineering for the 3D crossbar arrays and also provide an opportunity for all ZnO-based memory system in a low-temperature process. Furthermore, by increasing the ON/OFF ratio of ZnO/ZnWO$_x$ bilayer structure through process optimization and electrode/ZnO interface engineering, the ratio of R^{sneak}/R_{LRS} is expected be increased, thereby further enlarging the crossbar array numbers.[3]

4. CONCLUSIONS

We have demonstrated a spontaneous formation of ZnO/ZnWO$_x$ bilayer structure via interface engineering for the ReRAM application with multilevel storage operations. Not only a feasible study of multilevel storage operation for the ZnO/ZnWO$_x$ ReRAM device but also the performance of the ZnO/ZnWO$_x$-based CRS device with the voltage- and current-sweep modes were demonstrated and investigated in detail. The resistance switching behaviors of ZnO/ZnWO$_x$ bilayer ReRAM with adjustable RESET-stop voltages were explained using an electrochemical redox reaction model in terms of thermal activation energy, namely, Arrhenius equation whose thermal activation energies of 28, 40, and 133 meV for carriers hopping can be obtained at RESET-stop voltages of 1.0, 1.3, and 1.5 V, respectively. A DC endurance of at least 50 cycles at each RESET-stop voltage under the current-sweep mode shows a very stable multilevel operation. In addition, the measured values of resistance in the HRS were increased from 1.8 to 3.6 kΩ with the increase of RESET-stop voltage values from 2.0 to 2.4 V. The maximum array numbers (N) 9, 15, and 31 at RESET-stop voltages of 1.4, 1.5, and 1.6 V are estimated under the voltage-sweep mode, while the maximum array numbers are

increased into 47, 63, and 105 at RESET-stop voltages of 2.0, 2.2, and 2.4 V, under the current-sweep operation, respectively. Tunable multilevel storage of complementary resistive switching on single-step formation of ZnO/ZnWO$_x$ bilayer structure via interfacial engineering exhibits a promising potential for the 3D crossbar arrays. By increasing the ON/OFF ratio of ZnO/ZnWO$_x$ bilayer structure through process optimization and electrode/ZnO interface engineering, the ratio of R^{sneak}/R_{LRS} is expected to be increased, thereby further enlarging the crossbar array numbers.

■ ASSOCIATED CONTENT

ⓢ Supporting Information

Complementary resistive switching of A+B cells; operation of complementary resistive switching for two cells; degradation of ON-window with higher RESET-stop voltage through the voltage-sweep mode at negative and positive bias polarities; a schematic of N × N cross array with mistreating current path (sneak path). This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes
The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

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